CLAIMS

Please amend the claims as follows:

1. (Original) A method for merging vertical blanking intervals comprising:

storing a plurality of lines of data from a first service in a first memory (26) during a first write cycle;

storing a plurality of lines of data from a second service in a third memory (66) during the first write cycle;

storing a second plurality of lines of data from the first service in a second memory (30) during a second write cycle;

storing a second plurality of lines of data from the second service in a fourth memory (68) during the second write cycle;

reading selected lines of data in the second and fourth memories (30), (68) during the first write cycle; and

reading selected lines of the data in the first and third memories (26), 66) during the second write cycle.

2. (Original) The method of claim 1 wherein the memories (26), (30), (66), (68) are controlled by a controller (40).

3. (Original) The method of claim 2 wherein the controller (40) sends memory addresses to the memories (26), (30), (66), (68) during the write cycles to direct the data into selected memory locations.

4. (Original) The method of claim 3 wherein data is selected and read from locations in each memory (26), (30), (66), (68) according to addresses sent from the controller (40).

5. (Currently amended) An apparatus for merging video data comprising:

a controller (40);

first (26), second (30), third (66), and fourth (68) memories, responsive to said controller (40);

an input address bus (45), (49) connected between the controller (40) and the memories (26), (30), (66), (68);

an output address bus connected between the controller (40) and the memories (26), (30), (66), (68);

a first service input (22) connected to the first (26) and second (30) memories; ~~and~~

a second service input (65) connected to the third (66) and fourth (68) memories; ~~and~~

an output bus (59) connected to the first (26), second (30), third (66), and fourth (63) memories;

wherein the controller (40) stores data in the first (26) and third (66) memories while selectively reading data from the second (30) and fourth (68) memories during a first cycle and stores data in the second (30) and fourth (68) memories while selectively reading data from the first (26) and third (66) memories during a second cycle.

6. (Original) The apparatus according to claim 5 further comprising a plurality of control multiplexers (28), (32), (62), (63) operatively connected to the controller (40), each for controlling a respective one of the memories (26), (30), (66), (68).

7. (Original) The apparatus according to claim 5 wherein the controller (40) comprises a field programmable gate array.

8. (Original) The apparatus according to claim 5 further comprising an output data bus (59) connected to each of the memories (26), (30), (66), (68).

9. (Original) The apparatus according to claim 8 further comprising a first output multiplexer (34) operatively connected between the first (26) and second (30) memories.

10. (Original) The apparatus according to claim 9 further comprising a second output multiplexer (64) operatively connected to the first output multiplexer (34) and between the third (66) and fourth (68) memories.

11. (Original) The apparatus according to claim 8 further comprising a first input multiplexer (24) for directing data into the first (26) and second (30) memories.

12. (Original) The apparatus according to claim 11 further comprising a second input multiplexer for directing data into the third (66) and fourth (68) memories.

13. (Cancelled)

14. (Currently amended) The apparatus according to claim ~~13~~ 5 further comprising a plurality of control multiplexers (28), (32), (62), (63) operatively connected to each other and each being connected to a respective one of the memories (26), (30), (66), (68).

15. (Original) The apparatus according to claim 14 wherein said plurality of control multiplexers (28), (32), (62), (63) controls data flow in to and out of its respective memory (26), (30), (66), (68).

16. (Original) The apparatus according to claim 15 wherein said first output multiplexer (34) directs data out of the first (26) and second (30) memories to a common data bus (59).

17. (Original) The apparatus according to claim 16 wherein said second output multiplexer (64) directs data out of the third (66) and fourth (68) memories to the common data bus (59).